

W83194BR-703/W83194BG-703



STEPLESS CLOCK FOR SIS 741 CHIPSET

**W83194BR-703/W83194BG-703  
WINBOND CLOCK GENERATOR  
FOR SIS 741/964 CHIPSETS**

Date: Jan./23/2006      Revision: 0.8

# W83194BR-703/W83194BG-703



## W83194BR-703/W83194BG-703

### Data Sheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1					All of the versions before 0.50 are for internal use.
2	n.a.	09/03/2003	0.5	n.a.	First published preliminary version.
3	2,3,5, 6~14, 16~19	11/12/2003	0.6	n.a.	Delete some power manage pin, Add register, SRC fix 100MHz, Add AC/DC
4	2,3,6,8, 18	04/18/2004	0.7	n.a.	Correct IC version and default value
5		01/23/2006	0.8	n.a.	Add lead free part W83194BG-703
6					
7					
8					
9					
10					

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#### LIFE SUPPORT APPLICATIONS

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## 1. GENERAL DESCRIPTION

The W83194BR-703 is a Clock Synthesizer for SIS 741 chipset with 964 South Bridge. W83194BR-703 provides all clocks required for high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, PCI, and AGP clocks setting, support two ZCLK clock and one pair current mode differential SRC clock outputs; all clocks are externally selectable with smooth transitions.

The W83194BR-703 provides I<sup>2</sup>C serial bus interface to program the registers to enable or disable each clock outputs and provides -0.5% and +/-0.25% center type spread spectrum or programmable S.S.T. scale to reduce EMI.

The W83194BR-703 also has watchdog timer to support auto-reset when systems hanging caused by improper frequency setting.

The W83194BR-703 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply.

## 2. PRODUCT FEATURES

- 1 3.3V open drain Differential pairs clock outputs for CPU
- 1 3.3V open drain singled-ended clock output for chipset host bus.
- 1 pair 3.3V current mode differential SRC clock.
- 2 3.3V ZCLK clock outputs
- 2 AGP clock outputs
- 8 PCI synchronous clocks
- 2 2.5V IOAPIC clock outputs
- 1 24\_48Mhz clock output for super I/O.
- 1 12\_48 MHz clock output for USB.
- 3 14.318MHz REF clock outputs.
- ZCLK/AGP/PCI clock out supports synchronous and asynchronous mode
- Smooth frequency switch with selections from 100 to 218MHz
- Step-less frequency programming
- I<sup>2</sup>C 2-Wire serial interface and support byte read/write and block read/write.
- -0.5% and +/- 0.25% center type spread spectrum
- Programmable S.S.T. scale to reduce EMI
- Programmable registers to enable/stop each output and select modes
- Programmable clock outputs Skew control
- 48-pin SSOP package

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## 3. PIN CONFIGURATION

VDDREF	1	48	VDDI
FS0#/REF0	2	47	IOAPIC1
FS1#/REF1	3	46	IOAPIC0
REF2	4	45	GND
GND	5	44	VDDSRC
XIN	6	43	SRCT
XOUT	7	42	SRCC
GND	8	41	GND
ZCLK0	9	40	CPUT1
ZCLK1	10	39	GND
VDDZ	11	38	CPUT0
SCLK*	12	37	CPUC0
VDDPCI	13	36	VDDA
FS2*/PCI_F0	14	35	GND
FS3*/PCI_F1	15	34	IREF
PCI0	16	33	SDATA*
PCI1	17	32	GND
GND	18	31	AGP_0
VDDPCI	19	30	AGP_1
PCI2	20	29	VDDAGP
PCI3	21	28	VDD48
PCI4	22	27	12_48MHz/SEL12_48MHz#*
PCI5	23	26	24_48MHz^/SEL24_48MHz#&
GND	24	25	GND

#: Active low

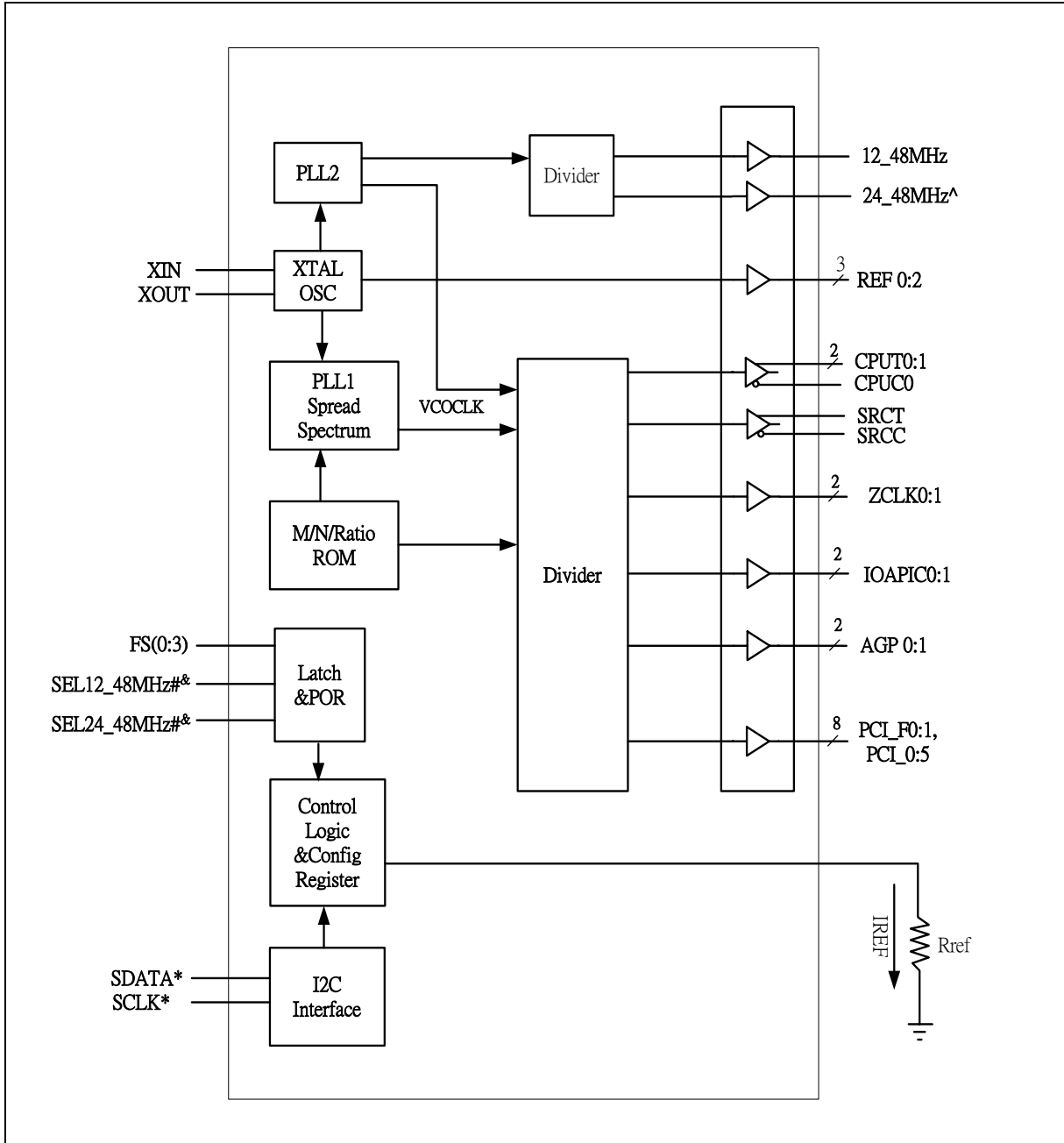
\*: Internal pull up resistor 120K to VDD

&: Internal Pull-down resistor 120K to GND

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## 4. BLOCK DIAGRAM



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## 5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
IN <sub>tp120k</sub>	Latched input at power up, internal 120kΩ pull up.
IN <sub>td120k</sub>	Latched input at power up, internal 120kΩ pull down.
OUT	Output
OD	Open Drain
#	Active Low
*	Internal 120kΩ pull-up
&	Internal 120 kΩ pull-down

### 5.1 Crystal I/O

PIN	PIN NAME	TYPE	DESCRIPTION
6	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
7	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors (18pF).

### 5.2 CPU, AGP, ZCLK and PCI, IOAPIC Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
38,37	CPUT0 CPUC0	OD	3.3V open drain differential clock outputs for AMD K7 CPU
40	CPUT1	OD	3.3V open drain singled –ended synchronize with CPUT0, For chipset host bus
43,42	SRCT, SRCC	OUT	Current mode differential clock outputs for SRC
31,30	AGP_0: 1	OUT	3.3V AGP clock outputs.
9,10	ZCLK0: 1	OUT	3.3V ZCLK clock outputs, For MuTIOL bus.
14	PCI_F0	OUT	3.3V PCI free running clock output.
	FS2*	IN <sub>tp120k</sub>	Latched input for FS2 at initial power up for H/W selecting the output frequency. This is internal 120K pull up.
15	PCI_F1	OUT	3.3V PCI free running clock output.
	FS3*	IN <sub>tp120k</sub>	Latched input for FS3 at initial power up for H/W selecting the output frequency, This is internal 120K pull up.
16,17,20,21 ,22,23	PCI [0:5]	OUT	Low skew (< 250ps) PCI clock outputs.
47,46	IOAPIC [0:1]	OUT	2.5V IOAPIC outputs.



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## 5.3 Fixed Frequency Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
2	REF0	OUT	14.318MHz output.
	FS0 <sup>&amp;</sup>	IN <sub>td120k</sub>	Latched input for FS0 at initial power up for H/W selecting the output frequency. This is internal 120K pull down.
3	REF1	OUT	14.318MHz output.
	FS1 <sup>&amp;</sup>	IN <sub>td120k</sub>	Latched input for FS1 at initial power up for H/W selecting the output frequency. This is internal 120K pull down.
4	REF2	OUT	14.318MHz output.
27	12_48MHz	OUT	12 MHz (default) or 48MHz clock output.
	SEL12_48MHz# <sup>*</sup>	IN <sub>tp120k</sub>	Latched input at initial power up for 12_48MHz output type selecting, SEL12_48MHz= 0 is 48 MHz, SEL12_48MHz=1 is 12MHz; This is internal 120KΩ pull up.
26	24_48MHz	OUT	24MHz or 48MHz (default) clock output.
	SEL24_48# <sup>&amp;</sup>	IN <sub>td120k</sub>	Latched input at initial power up for 24_48MHz output type selecting, SEL24_48MHz= 0 is 48 MHz, SEL24_48MHz=1 is 24MHz; This is internal 120KΩ pull down.

## 5.4 I2C Control Interface

PIN	PIN NAME	TYPE	DESCRIPTION
33	SDATA <sup>*</sup>	I/OD	Serial data of I <sup>2</sup> C 2-wire control interface with internal pull-up resistor.
12	SCLK <sup>*</sup>	IN	Serial clock of I <sup>2</sup> C 2-wire control interface with internal pull-up resistor.

## 5.5 Power Management Pins

PIN	PIN NAME	TYPE	DESCRIPTION															
34	IREF	OUT	Deciding the reference current for the SRCT/C pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current. The table is show as follows.															
			<table border="1"> <thead> <tr> <th>MULTSEL (PIN 11)</th> <th>Board Target Trace/ Term Z</th> <th>Reference R, Iref=VDD/(3*Rr )</th> <th>Output Current</th> <th>Ioh @ Z</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>50 Ohms</td> <td>R=475 1% Iref=2.32mA</td> <td>Ioh= 6*Iref</td> <td>0.7V @ 50</td> </tr> <tr> <td>0</td> <td>50 Ohms</td> <td>R=221 1% Iref=5mA</td> <td>Ioh= 4*Iref</td> <td>1.0V @ 50</td> </tr> </tbody> </table>	MULTSEL (PIN 11)	Board Target Trace/ Term Z	Reference R, Iref=VDD/(3*Rr )	Output Current	Ioh @ Z	1	50 Ohms	R=475 1% Iref=2.32mA	Ioh= 6*Iref	0.7V @ 50	0	50 Ohms	R=221 1% Iref=5mA	Ioh= 4*Iref	1.0V @ 50
			MULTSEL (PIN 11)	Board Target Trace/ Term Z	Reference R, Iref=VDD/(3*Rr )	Output Current	Ioh @ Z											
1	50 Ohms	R=475 1% Iref=2.32mA	Ioh= 6*Iref	0.7V @ 50														
0	50 Ohms	R=221 1% Iref=5mA	Ioh= 4*Iref	1.0V @ 50														

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### 5.6 Power Pins

PIN	PIN NAME	TYPE	DESCRIPTION
1	VDDREF	PWR	3.3V power supply for REF.
13,19	VDDPCI	PWR	3.3V power supply for PCI.
29	VDDAGP	PWR	3.3V power supply for AGP.
44	VDDSRC	PWR	2.5V power supply for SRC.
28	VDD48	PWR	3.3V power supply for 48MHz.
11	VDDZ	PWR	3.3V power supply for ZCLK.
48	VDDI	PWR	2.5V power supply for IOAPIC
36	VDDA	PWR	3.3V power supply for Analog core logic.
5,8,18,24,25,32, 35,39,41,45	GND	PWR	Ground pin

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## 6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [4:0] value or software programming at SSEL [4:0] (Register 0 bit 7 ~ 3).

FS4	FS3	FS2	FS1	FS0	CPU (MHZ)	SRC (MHZ)	ZCLK (MHZ)	AGP (MHZ)	PCI (MHZ)
0	0	0	0	0	200.00	100.00	133.33	66.67	33.33
0	0	0	0	1	200.00	100.00	133.33	66.67	33.33
0	0	0	1	0	200.99	100.00	133.99	67.00	33.50
0	0	0	1	1	190.00	100.00	126.67	63.33	31.67
0	0	1	0	0	100.00	100.00	133.33	66.67	33.33
0	0	1	0	1	100.00	100.00	133.33	66.67	33.33
0	0	1	1	0	100.99	100.00	134.65	67.33	33.66
0	0	1	1	1	95.00	100.00	126.67	63.33	31.67
0	1	0	0	0	160.00	100.00	133.33	66.67	33.33
0	1	0	0	1	166.66	100.00	138.88	69.44	34.72
0	1	0	1	0	161.58	100.00	134.65	67.33	33.66
0	1	0	1	1	152.00	100.00	126.67	63.33	31.67
0	1	1	0	0	133.33	100.00	133.33	66.67	33.33
0	1	1	0	1	133.33	100.00	133.33	66.67	33.33
0	1	1	1	0	133.99	100.00	133.99	67.00	33.50
0	1	1	1	1	126.66	100.00	126.66	63.33	31.67
1	0	0	0	0	206.00	100.00	137.33	68.67	34.33
1	0	0	0	1	210.00	100.00	140.00	70.00	35.00
1	0	0	1	0	214.00	100.00	142.67	71.33	35.67
1	0	0	1	1	218.00	100.00	145.33	72.67	36.33
1	0	1	0	0	103.00	100.00	137.33	68.67	34.33
1	0	1	0	1	105.00	100.00	140.00	70.00	35.00
1	0	1	1	0	107.00	100.00	142.67	71.33	35.67
1	0	1	1	1	109.00	100.00	145.33	72.67	36.33
1	1	0	0	0	164.80	100.00	137.33	68.67	34.33
1	1	0	0	1	168.00	100.00	140.00	70.00	35.00
1	1	0	1	0	171.20	100.00	142.67	71.33	35.67
1	1	0	1	1	174.40	100.00	145.33	72.67	36.33
1	1	1	0	0	137.33	100.00	137.33	68.67	34.33
1	1	1	0	1	140.00	100.00	140.00	70.00	35.00
1	1	1	1	0	142.67	100.00	142.67	71.34	35.67
1	1	1	1	1	145.33	100.00	145.33	72.67	36.33



## 7. I<sup>2</sup>C CONTROL AND STATUS REGISTERS

### 7.1 Register 0: Frequency Select (Default = 20h)

BIT	NAME	PWD	DESCRIPTION
7	SSEL [4]	0	Frequency selection by software via I <sup>2</sup> C
6	SSEL [3]	0	
5	SSEL [2]	1	
4	SSEL [1]	0	
3	SSEL [0]	0	
2	EN_SSEL	0	Enable software table selection FS [4:0]. 0 = Hardware table setting (Jump mode). 1 = Software table setting through Bit7~3. (Jump less mode)
1	EN_SPSP	0	Enable spread spectrum mode under clock output. 0 = Spread Spectrum mode disable 1 = Spread Spectrum mode enable
0	EN_SAFE_FREQ	0	After watchdog timeout 0 = Reload the hardware FS [4:0] latched pins setting. 1 = Reload the desirable frequency table selection defined at Reg-5 Bit 4~0.

### 7.2 Register 1: CPU Control (1 = Enable, 0 = Stopped) (Default: ECh)

BIT	PIN NO	PWD	DESCRIPTION
7	Reserved	1	Reserved
6	40	1	CPUT1 output control
5	38,37	1	CPUT0 / C0 output control
4	Reserved	X	Reserved. Default: 0 (Read only)
3	15	X	Power on latched value of FS3 pin. Default: 1 (Read only)
2	14	X	Power on latched value of FS2 pin. Default: 1 (Read only)
1	3	X	Power on latched value of FS1 pin. Default: 0 (Read only)
0	2	X	Power on latched value of FS0 pin. Default: 0 (Read only)

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### 7.3 Register 2: PCI, ZCLK Control (1 = Enable, 0 = Stopped) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION
7	-	1	Reserved
6	15	1	PCI_F1 output control
5	14	1	PCI_F0 output control
4	10	1	ZCLK1 output control
3	9	1	ZCLK0 output control
2	23	1	PCI5 output control
1	22	1	PCI4 output control
0	21	1	PCI3 output control

### 7.4 Register 3: PCI, AGP Control (1 = Enable, 0 = Stopped) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION
7	20	1	PCI2 output control
6	17	1	PCI1 output control
5	16	1	PCI0 output control
4	SEL12_48	X	12_48 MHz output selection, 1: 12 MHz (default) 0: 48 MHz. Default value follow hardware trapping data on SEL12_48# pin.
3	47	1	IOAPIC1 output control
2	46	1	IOAPIC0 output control
1	30	1	AGP_1 output control
0	31	1	AGP_0 output control

### 7.5 Register 4: 48MHz, REF, SRC Control (1 = Enable, 0 = Stopped) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION
7	26	1	24_48MHz output control
6	27	1	12_48MHz output control
5	-	1	Reserved
4	4	1	REF2 output control
3	3	1	REF1 output control
2	2	1	REF0 output control
1	47,46	1	SRC output control
0	-	1	Reserved

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### 7.6 Register 5: Watchdog Control (Default: 04h)

BIT	NAME	PWD	DESCRIPTION
7	SEL24_48	X	24 / 48 MHz output selection, 1: 24 MHz 0: 48 MHz (Default), Default value follow hardware trapping data on SEL24_48# pin.
6	CNT_EN	0	Program this bit => 1: Enable Watchdog Timer feature. 0: Disable Watchdog Timer feature. Read-back this bit => During timer count down the bit read back to 1. If count to zero, this bit read back to 0.
5	WD_TIMEOUT	0	Read Back only. Timeout Flag. This bit is Read Only. 1: Watchdog has ever started and counts to zero. 0: Watchdog is restarted and counting.
4	SAF_FREQ [4]	0	These bits will be reloaded in Reg-0 to select frequency table. As the watchdog is timeout and EN_SAFE_FREQ=1.
3	SAF_FREQ [3]	0	
2	SAF_FREQ [2]	1	
1	SAF_FREQ [1]	0	
0	SAF_FREQ [0]	0	

### 7.7 Register 6: Skew Control (Default: 25h)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	0	Reserved
6	Reserved	0	Reserved
5	Reserved	1	Reserved
4	Reserved	0	
3	Reserved	0	
2	CSKEW<2>	1	CPU1 to CPU0 skew control
1	CSKEW<1>	0	Skew resolution is 250ps
0	CSKEW<0>	1	The decision of skew direction is same as CSKEW<2:0> setting

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### 7.8 Register 7: Winbond Chip ID (Default: 77h) (Read only)

BIT	NAME	PWD	DESCRIPTION
7	CHPI_ID [7]	0	Winbond Chip ID. W83194BR-703 (SA5877).
6	CHPI_ID [6]	1	Winbond Chip ID.
5	CHPI_ID [5]	1	Winbond Chip ID.
4	CHPI_ID [4]	1	Winbond Chip ID.
3	CHPI_ID [3]	0	Winbond Chip ID.
2	CHPI_ID [2]	1	Winbond Chip ID.
1	CHPI_ID [1]	1	Winbond Chip ID.
0	CHPI_ID [0]	1	Winbond Chip ID.

### 7.9 Register 8: M/N (Default: 90h)

BIT	NAME	PWD	DESCRIPTION
7	NVAL<8>	X	Programmable N divisor value. Bit 7 ~0 are defined in the Register 9.  Programmable M divisor
6	MVAL<6>	X	
5	MVAL<5>	X	
4	MVAL<4>	X	
3	MVAL<3>	X	
2	MVAL<2>	X	
1	MVAL<1>	X	
0	MVAL<0>	X	

### 7.10 Register 9: N (Default: BBh)

BIT	NAME	PWD	DESCRIPTION
7	NVAL<7>	X	Programmable N divisor bit 7 ~0. The bit 8 is defined in Register 8, The bit 9 is defined in Register 10
6	NVAL<6>	X	
5	NVAL<5>	X	
4	NVAL<4>	X	
3	NVAL<3>	X	
2	NVAL<2>	X	
1	NVAL<1>	X	
0	NVAL<0>	X	

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## 7.11 Register 10: N & N3 (Default: 3Bh)

BIT	NAME	PWD	DESCRIPTION
7	NVAL<9>	X	Programmable N divisor bit 9.
6	N3VAL<6>	X	Programmable N3 divisor bit 6 ~0 for programmable SRC clock. PS: Frequency range: 86.8M ~ 115.2M Resolution: 224K
5	N3VAL<5>	X	
4	N3VAL<4>	X	
3	N3VAL<3>	X	
2	N3VAL<2>	X	
1	N3VAL<1>	X	
0	N3VAL<0>	X	

## 7.12 Register 11: Spread Spectrum Programming (Default: 0Eh)

BIT	NAME	PWD	DESCRIPTION
7	SP_UP [3]	0	Spread Spectrum Up Counter bit 3 ~ bit 0.
6	SP_UP [2]	0	
5	SP_UP [1]	0	
4	SP_UP [0]	0	
3	SP_DOWN [3]	1	Spread Spectrum Down Counter bit 3 ~ bit 0 2's complement representation. Ex: 1 -> 1111; 2 -> 1110; 7 -> 1001; 8 -> 1000
2	SP_DOWN [2]	1	
1	SP_DOWN [1]	1	
0	SP_DOWN [0]	0	

## 7.13 Register 12: Divisor and Step-less Enable Control (Default: 89h)

BIT	NAME	PWD	DESCRIPTION
7	M_NACC_EN	1	Enable variable accumulation period for M divisor 1: Enable, 0: Disable (Original timing)
6	KVAL<9>	X	Define the ZCLK divider ratio
5	KVAL<5>	X	Table-2 integrate the all divider configuration
4	Reserved	X	Reserved
3	Reserved	X	
2	KVAL<2>	X	Define the CPU divider ratio
1	KVAL<1>	X	Refer to Table-2
0	KVAL<0>	X	





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### 7.15 Register 14: Spread Spectrum Control (Default: 10h)

BIT	NAME	PWD	DESCRIPTION
7	CPUT_DRI	0	CPUT output state in during POWER DOWN or Stop mode assertion. 1: Driven (2*Iref) 0: Tristate (Floating) CPUC always tri-state (floating) in power down Assertion.
6	SRCT_DRI	0	SRC_T output state in during POWER DOWN or Stop mode assertion. 1: Driven (6*Iref => STOP mode) (2*Iref => POWER DOWN) 0: Tristate (Floating) SRC_C always tri-state (floating) in power down Assertion.
5	SPCNT<5>	0	Spread Spectrum Programmable time, the resolution is 280ns. Default period is 11.8us
4	SPCNT<4>	1	
3	SPCNT<3>	0	
2	SPCNT<2>	0	
1	SPCNT<1>	0	
0	SPCNT<0>	0	

### 7.16 Register 15: Spread Spectrum type Control (Default: 2Ch)

BIT	NAME	PWD	DESCRIPTION
7	INV_CPU	0	Invert the CPU phase, 0: Default, 1: Inverse
6	INV_ZCLK	0	Invert the ZCLK phase, 0: Default, 1: Inverse
5	Reserved	1	Reserved
4	SPSP1	0	Spread Spectrum type select.
3	SPSP0	1	00: Down 1% 01: Down 0.5% 10: Center +/- 0.5% 11: Center +/- 0.25%
2	ASKEW<2>	1	CPU1 to AGP skew control.
1	ASKEW<1>	0	Skew resolution is 250ps
0	ASKEW<0>	0	The decision of skew direction is same as ASKEW<2:0> setting

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## 7.17 Register 16: Skew Control (Default: 24h)

Bit	Name	PWD	Description
7	INV_AGP	0	Invert the AGP phase, 0: Default, 1: Inverse
6	INV_PCI	0	Invert the PCI phase, 0: Default, 1: Inverse
5	ZSKEW<2>	1	CPU1 to ZCLK skew control
4	ZSKEW<1>	0	Skew resolution is 250ps
3	ZSKEW<0>	0	The decision of skew direction is same as ZSKEW<2:0> setting
2	PSKEW<2>	1	CPU1 to PCI skew control
1	PSKEW<1>	0	Skew resolution is 250ps
0	PSKEW<0>	0	The decision of skew direction is same as PSKEW<2:0> setting

## 7.18 Register 17: Slew rate Control (Default: 00h)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	0	Reserved
6	INV_USB12	0	Invert the USB12_48 phase, 0: In phase with USB24_48 1: 180 degrees out of phase
5	PCI_F0_S2	0	PCI_F1 / PCI_F0 slew rate control
4	PCI_F0_S1	0	11: Strong, 00: Weak, 10/01: Normal
3	IOAPIC_S2	0	IOAPIC1, 0 slew rate control
2	IOAPIC_S1	0	11: Strong, 00: Weak, 10/01: Normal
1	AGP_10_S2	0	AGP_1 / AGP_0 slew rate control
0	AGP_10_S1	0	11: Strong, 00: Weak, 10/01: Normal

## 7.19 Register 18: Slew rate Control (Default: 00h)

BIT	NAME	PWD	DESCRIPTION
7	PCI_5_S2	0	PCI5 slew rate control
6	PCI_5_S1	0	11: Strong, 00: Weak, 10/01: Normal
5	PCI_42_S2	0	PCI4, 3,2 slew rate control
4	PCI_42_S1	0	11: Strong, 00: Weak, 10/01: Normal
3	PCI_10_S2	0	PCI1, 0 slew rate control
2	PCI_10_S1	0	11: Strong, 00: Weak, 10/01: Normal
1	REF_S2	0	REF0, 1, 2 slew rate control
0	REF_S1	0	11: Strong, 00: Weak, 10/01: Normal

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### 7.20 Register 19: Slew rate Control (Default: D2h)

BIT	NAME	PWD	DESCRIPTION
7	CPU1S_EN	1	Stop CPU1 clocks, 1: Enable stop feature, 0: Disable
6	CPU0S_EN	1	Stop CPU0 clocks, 1: Enable stop feature, 0: Disable
5	ZCLK_S2	0	ZCLK1, 0 slew rate control
4	ZCLK_S1	1	11: Strong, 00: Weak, 10/01: Normal
3	INV_USB48	0	Invert the USB48 phase 0: In phase with USB24_48 1: 180 degrees out of phase
2	USB48_S2	0	USB48/USB12_48/USB24_48 slew rate control
1	USB48_S1	1	11: Strong, 00: Weak, 10/01: Normal
0	Reserved	0	Reserved

### 7.21 Register 20: SRC select Control (Default: 88h)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	1	Reserved for test only please don't modify it.
6	SEC<6>	0	Setting the down count depth. One bit resolution Represent 250ms. Default time depth is 8*250ms = 2.0 second. If the watchdog timer is counting, this register will return present down count value.
5	SEC<5>	0	
4	SEC<4>	0	
3	SEC<3>	1	
2	SEC<2>	0	
1	SEC<1>	0	
0	SEC<0>	0	

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## 7.22 Register 21: Fix Mode Control (Default: 00h)

BIT	NAME	PWD	DESCRIPTION								
7	TRI-EN	0	Tri-state all output if set 1								
6	FIX_ZCLK	0	ZCLK output frequency select mode (Only valid under FIX_ADDR<2:0> is nonzero) 0: Output frequency according to frequency selection table 1: Output frequency according to FIX frequency table								
5	FIX_PCI	0	PCI output frequency select mode (Only valid under FIX_ADDR<2:0> is nonzero) 0: Output frequency according to frequency selection table 1: Output frequency according to FIX frequency table								
4	FIX_AGP	0	AGP output frequency select mode (Only valid under FIX_ADDR<2:0> is nonzero) 0: Output frequency according to frequency selection table 1: Output frequency according to FIX frequency table								
3	Reserved	0	Reserved for test only please don't modify it.								
2	FIX_ADDR<2>	0	Asynchronous ZCLK/AGP/PCI frequency table selection								
1	FIX_ADDR<1>	0									
0	FIX_ADDR<0>	0	<table border="0"> <tr> <td>001: 132 / 66 / 33M</td> <td>010:132 / 75.43 / 37.7M</td> </tr> <tr> <td>011: 132 / 88 / 44M</td> <td>100:176 / 88 / 44M</td> </tr> <tr> <td>101: 132 / 66 / 33M</td> <td>110:132 / 75.43 / 33M</td> </tr> <tr> <td>111: 132 / 88 / 33M</td> <td>000: Clock from PLL1</td> </tr> </table>	001: 132 / 66 / 33M	010:132 / 75.43 / 37.7M	011: 132 / 88 / 44M	100:176 / 88 / 44M	101: 132 / 66 / 33M	110:132 / 75.43 / 33M	111: 132 / 88 / 33M	000: Clock from PLL1
001: 132 / 66 / 33M	010:132 / 75.43 / 37.7M										
011: 132 / 88 / 44M	100:176 / 88 / 44M										
101: 132 / 66 / 33M	110:132 / 75.43 / 33M										
111: 132 / 88 / 33M	000: Clock from PLL1										

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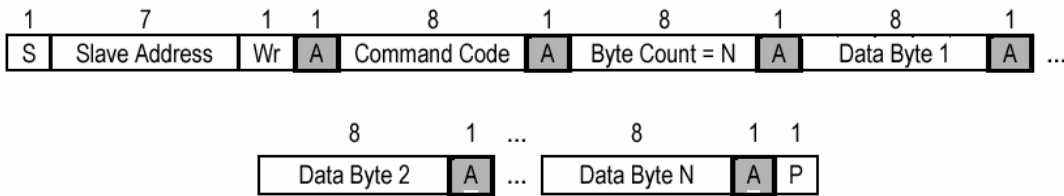


## 8. ACCESS INTERFACE

The W83194BR-703 provides I<sup>2</sup>C Serial Bus for microprocessor to read/write internal registers. In the W83194BR-703 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I<sup>2</sup>C address is defined at 0xD2.

Block Read and Block Write Protocol

### 8.1 Block Write protocol

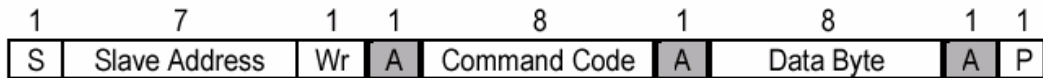


### 8.2 Block Read protocol

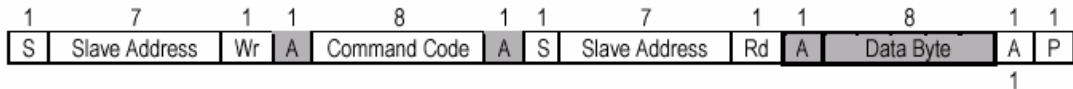


## In block mode, the command code must filled 8'h00

### 8.3 Byte Write protocol



### 8.4 Byte Read protocol



# W83194BR-703/W83194BG-703



## 9. SPECIFICATIONS

### 9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

PARAMETER	RATING
Absolute 3.3V Core Supply Voltage	-0.5V to +4.6V
Absolute 3.3V I/O Supply Voltage	- 0.5 V to + 4.6 V
Operating 3.3V Core Supply Voltage	3.135V to 3.465V
Operating 3.3V I/O Supply Voltage	3.135V to 3.465V
Storage Temperature	- 65°C to + 150°C
Ambient Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Input ESD protection (Human body model)	2000V

### 9.2 General Operating Characteristics

<b>VDD48=VDDAGP=VDDREF=VDDPCI= 3.3V ± 5 %, TA = 0°C to +70°C, CI=10pF</b>					
PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V <sub>IL</sub>		0.8	V <sub>dc</sub>	
Input High Voltage	V <sub>IH</sub>	2.0		V <sub>dc</sub>	
Output Low Voltage	V <sub>OL</sub>		0.4	V <sub>dc</sub>	All outputs using 3.3V power
Output High Voltage	V <sub>OH</sub>	2.4		V <sub>dc</sub>	All outputs using 3.3V power
Operating Supply Current	I <sub>dd</sub>		350	mA	CPU = 100 to 200 MHz PCI = 33.3 Mhz with load
Input pin capacitance	C <sub>in</sub>		5	pF	
Output pin capacitance	C <sub>out</sub>		6	pF	
Input pin inductance	L <sub>in</sub>		7	nH	

### 9.3 Skew Group timing clock

<b>VDD48=VDDAGP=VDDREF=VDDPCI= 3.3V ± 5 %, TA = 0°C to +70°C, CI=10pF</b>					
PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
AGP to PCI Skew	1.5	2.6	3.5	ns	Measured at 1.5V
CPU to CPU Skew			200	ps	Crossing point
AGP to AGP Skew			250	ps	Measured at 1.5V
PCI to PCI Skew			500	ps	Measured at 1.5V
48MHz to 48MHz Skew			1000	ps	Measured at 1.5V
REF to REF Skew			500	ps	Measured at 1.5V

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### 9.4 CPU (Open Drain) Electrical Characteristics

<i>TA = 0°C to +70°C, external 1.5V pull-up</i>				
Parameter	Min	Max	Units	Test Conditions
Rise Time	-	900	ps	100 to 200 Mhz, Vol=20%, Voh=80%
Fall Time	-	900	ps	100 to 200Mhz, Vol=20%, Voh=80%
Absolute crossing point Voltages	550	1250	mV	100 to 200Mhz
Cycle to Cycle jitter		250	ps	100 to 200Mhz
Duty Cycle	45	55	%	100 to 200Mhz

### 9.5 SRC 0.7V Electrical Characteristics

<i>VDDSRC= 3.3V ± 5 %, TA = 0°C to +70°C,</i>				
PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
Rise Time	175	700	ps	100 Mhz , Measure from Vol=0.175 to Voh=0.525
Fall Time	175	700	ps	100 Mhz, Measure from Vol=0.175 to Voh=0.525
Absolute crossing point Voltages	250	550	mV	100 Mhz
Cycle to Cycle jitter		125	ps	100 Mhz, Measure from differential waveform
Duty Cycle	45	55	%	100 Mhz, Measure from differential waveform

### 9.6 AGP, ZCLK Electrical Characteristics

<i>VDDAGP= 3.3V ± 5 %, TA = 0°C to +70°C, Test load, Cl=10pF,</i>				
PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
Rise Time	500	2000	ps	Measure from 0.4V to 2.4V
Fall Time	500	2000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		250	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V



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## 9.7 PCI Electrical Characteristics

<b>VDDPCI= 3.3V ± 5 %, TA = 0°C to +70°C, Test load, CI=10pF,</b>				
<b>PARAMETER</b>	<b>MIN</b>	<b>MAX</b>	<b>UNITS</b>	<b>TEST CONDITIONS</b>
Rise Time	500	2000	ps	Measure from 0.4V to 2.4V
Fall Time	500	2000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		250	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

## 9.8 24M, 48M Electrical Characteristics

<b>VDD48= 3.3V ± 5 %, TA = 0°C to +70°C, Test load, CI=10pF,</b>				
<b>PARAMETER</b>	<b>MIN</b>	<b>MAX</b>	<b>UNITS</b>	<b>TEST CONDITIONS</b>
Rise Time	500	2000	ps	Measure from 0.4V to 2.4V
Fall Time	500	2000	ps	Measure from 2.4V to 0.4V
Long term jitter		500	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

## 9.9 REF Electrical Characteristics

<b>VDDREF= 3.3V ± 5 %, TA = 0°C to +70°C, Test load, CI=10pF,</b>				
<b>PARAMETER</b>	<b>MIN</b>	<b>MAX</b>	<b>UNITS</b>	<b>TEST CONDITIONS</b>
Rise Time	1000	4000	ps	Measure from 0.4V to 2.4V
Fall Time	1000	4000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		1000	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

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### 9.10 IOAPIC Electrical Characteristics

<i>VDDI= 2.5V ± 5 %, TA = 0°C to +70°C, Test load, Cl=10pF,</i>				
PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
Rise Time	400	1600	ps	Measure from 0.4V to 2.0V
Fall Time	400	1600	ps	Measure from 2.0V to 0.4V
Cycle to Cycle jitter		500	ps	Measure 1.25V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-27		mA	Vout=1.0V
Pull-Up Current Max		-27	mA	Vout=2.375V
Pull-Down Current Min	27		mA	Vout=1.2V
Pull-Down Current Max		30	mA	Vout=0.3V

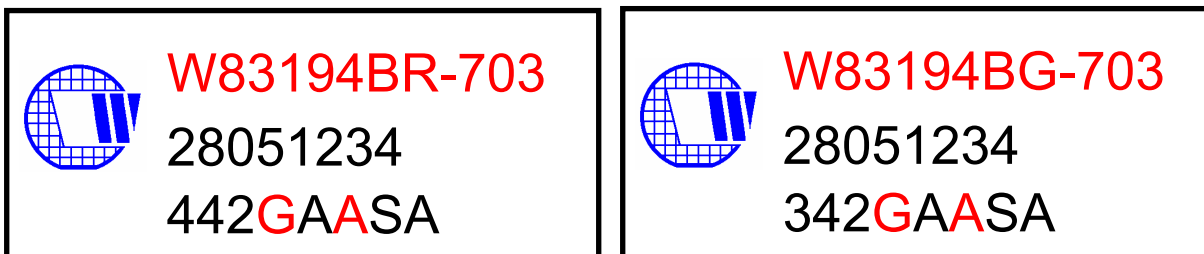
### 10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83194BR-703	48 PIN SSOP	Commercial, 0°C to +70°C
W83194BG-703	48 PIN SSOP (Lead free package)	Commercial, 0°C to +70°C

## W83194BR-703/W83194BG-703



### 11. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number:

Normal part :W83194BR-703, Lead free part: W83194BG-703

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 342 G A A SA

442: packages made in '2004, week 42

G: assembly house ID; O means OSE, G means GR

A: Internal use code

A: IC revision

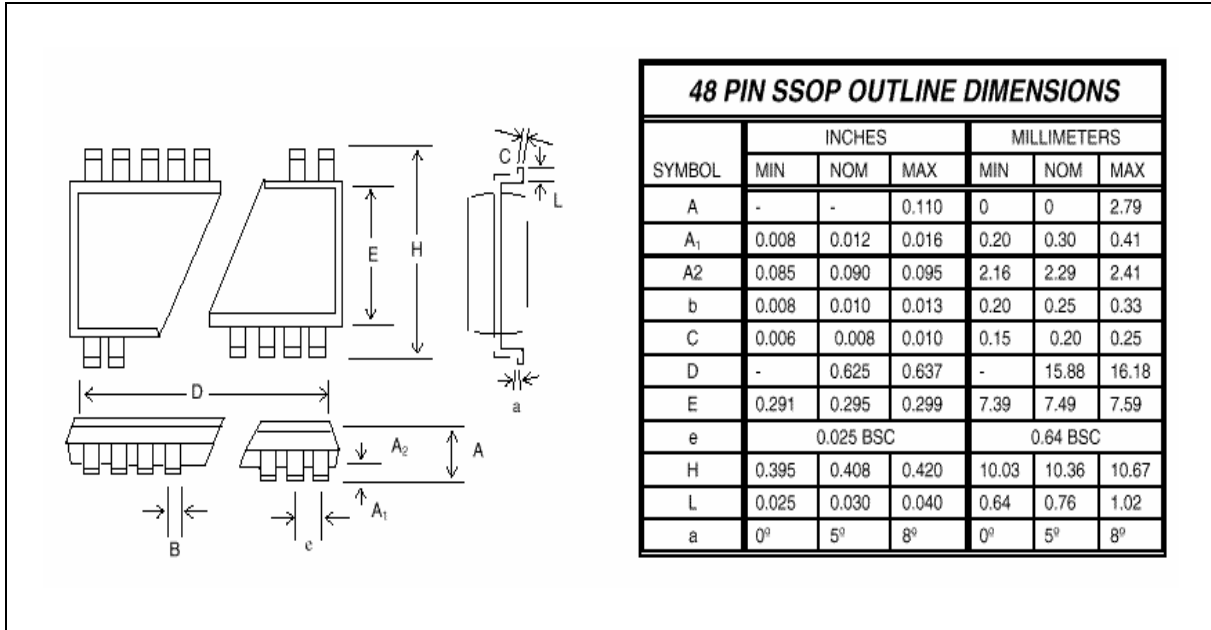
SA: mask version

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# W83194BR-703/W83194BG-703



## 12. PACKAGE DRAWING AND DIMENSIONS



### Important Notice

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